

Docket No.: GR 00 P 4121

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By: [Signature]

Date: 6/18/01

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : Albert Birner et al.  
Applic. No. : 09/871,013  
Filed : May 31, 2001  
Title : Method For Making Electrical Contact With A Rear Side Of A  
Semiconductor Substrate During Its Processing

INFORMATION DISCLOSURE STATEMENT

Hon. Commissioner of Patents and Trademarks,  
Washington, D.C. 20231

Sir:

In accordance with 37 C.F.R. 1.98 copies of the following patents and/or publications are submitted herewith:

U.S. Patent No. 4,428,815 (Powell et al.), dated January 31, 1984;

U.S. Patent No. 5,209,833 (Foell et al.), dated May 11, 1993;

U.S. Patent No. 5,437,777 (Kishi), dated August 1, 1995;

German Published, Non-Prosecuted Application DE 197 28 962 A1 (Kretschmer et al.), dated January 7, 1999, device for etching a semiconductor wafer;

Published Japanese Patent Abstract JP 59041830 A (Setsuo), dated March 8, 1984;


Published Japanese Patent Abstract JP 62293632 A (Hironori et al.), dated December 21, 1987;

Published Japanese Patent Abstract JP 10046394 A (Fumihiro et al.), dated February 17, 1998;

Published Japanese Patent Abstract JP 11181600 A (Junichiro et al.), dated July 6, 1999

If no translation of pertinent portions of any foreign language patents or publications mentioned above is included with the aforementioned copies of those applications, patents and/or publications, it is because no existing translation is readily available to the applicant.

Respectfully submitted,

  
For Applicants

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Date: June 18, 2001

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